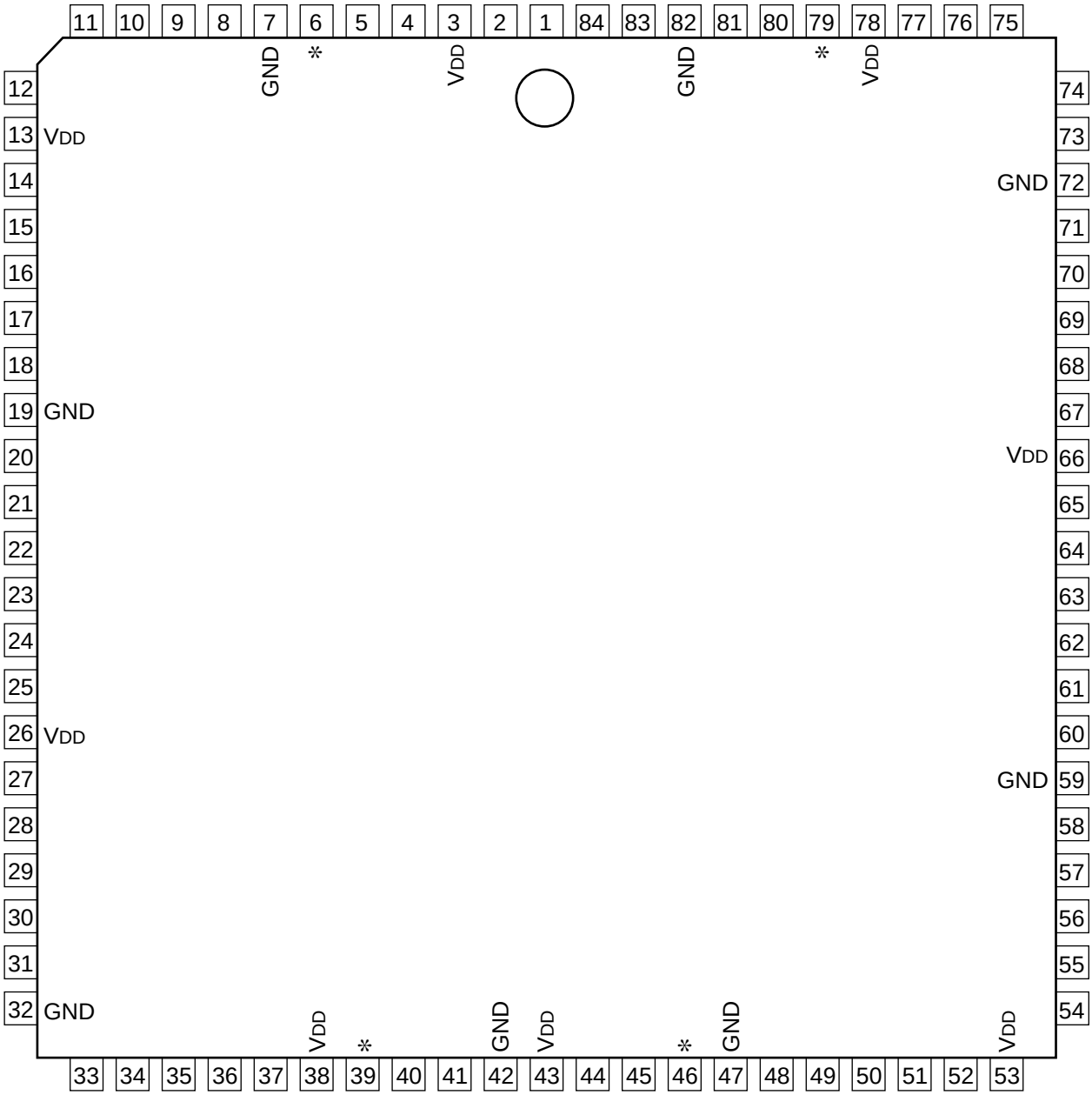
C-MOS ELECTRICAL ERASABLE PLD

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	GCLR	22	I/O	LAB B	43	—	VDD	64	I/O	LAB G
2	I	OE2	23	I/O	LAB C	44	I/O	LAB E	65	I/O	LAB G
3	—	VDD	24	I/O	LAB C	45	I/O	LAB E	66	—	VDD
4	I/O	LAB A	25	I/O	LAB C	46	I/O	LAB E*	67	I/O	LAB G
5	I/O	LAB A	26	—	VDD	47	—	GND	68	I/O	LAB G
6	I/O	LAB A*	27	I/O	LAB C	48	I/O	LAB E	69	I/O	LAB G
7	—	GND	28	I/O	LAB C	49	I/O	LAB E	70	I/O	LAB G
8	I/O	LAB A	29	I/O	LAB C	50	I/O	LAB E	71	I/O	LAB G
9	I/O	LAB A	30	I/O	LAB C	51	I/O	LAB E	72	—	GND
10	I/O	LAB A	31	I/O	LAB C	52	I/O	LAB E	73	I/O	LAB H
11	I/O	LAB A	32	—	GND	53	—	VDD	74	I/O	LAB H
12	I/O	LAB A	33	I/O	LAB D	54	I/O	LAB F	75	I/O	LAB H
13	—	VDD	34	I/O	LAB D	55	I/O	LAB F	76	I/O	LAB H
14	I/O	LAB B	35	I/O	LAB D	56	I/O	LAB F	77	I/O	LAB H
15	I/O	LAB B	36	I/O	LAB D	57	I/O	LAB F	78	—	VDD
16	I/O	LAB B	37	I/O	LAB D	58	I/O	LAB F	79	I/O	LAB H*
17	I/O	LAB B	38	—	VDD	59	—	GND	80	I/O	LAB H
18	I/O	LAB B	39	I/O	LAB D*	60	I/O	LAB F	81	I/O	LAB H
19	—	GND	40	I/O	LAB D	61	I/O	LAB F	82	—	GND
20	I/O	LAB B	41	I/O	LAB D	62	I/O	LAB F	83	I	GCLK
21	I/O	LAB B	42	—	GND	63	I/O	LAB G	84	I	OE1

INPUT

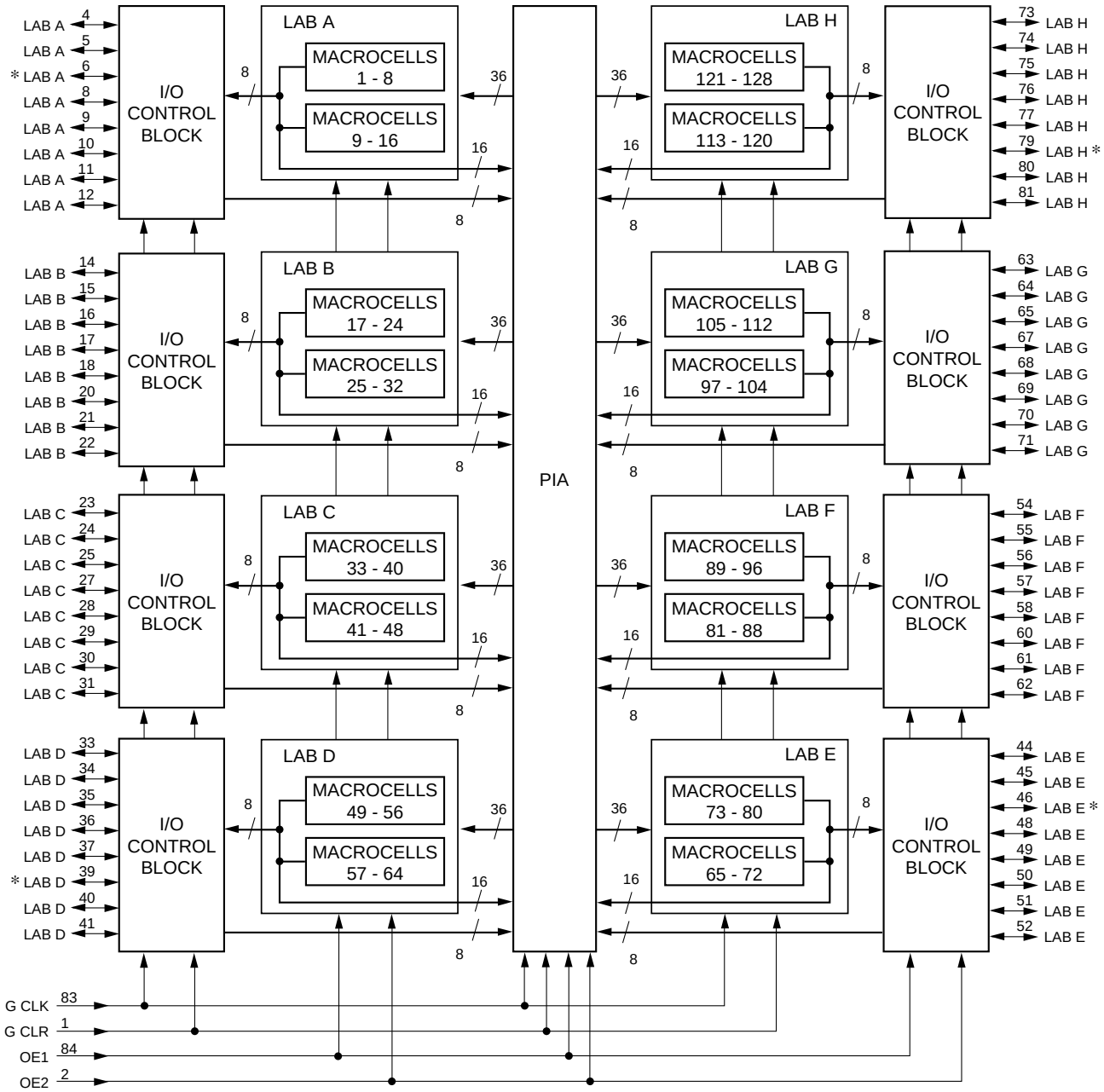
GCLK : GROBAL CLOCK
GCLR : GROBAL CLEAR
OE1, 2 : OUTPUT ENABLE 1, 2

INPUT/OUTPUT

LAB A : LOGIC ARRAY BLOCK A
LAB B : LOGIC ARRAY BLOCK B
LAB C : LOGIC ARRAY BLOCK C
LAB D : LOGIC ARRAY BLOCK D
LAB E : LOGIC ARRAY BLOCK E
LAB F : LOGIC ARRAY BLOCK F
LAB G : LOGIC ARRAY BLOCK G
LAB H : LOGIC ARRAY BLOCK H

NOTE

* : No CONNECT
(EPM7160E)



NOTE
∗ : No CONNECT (EPM7160E)